EXHIBIT I

U.S. Patent No. 6,797,572

TSMC Products
(TSMC 20nm and 28nm HKMG integrated circuit)

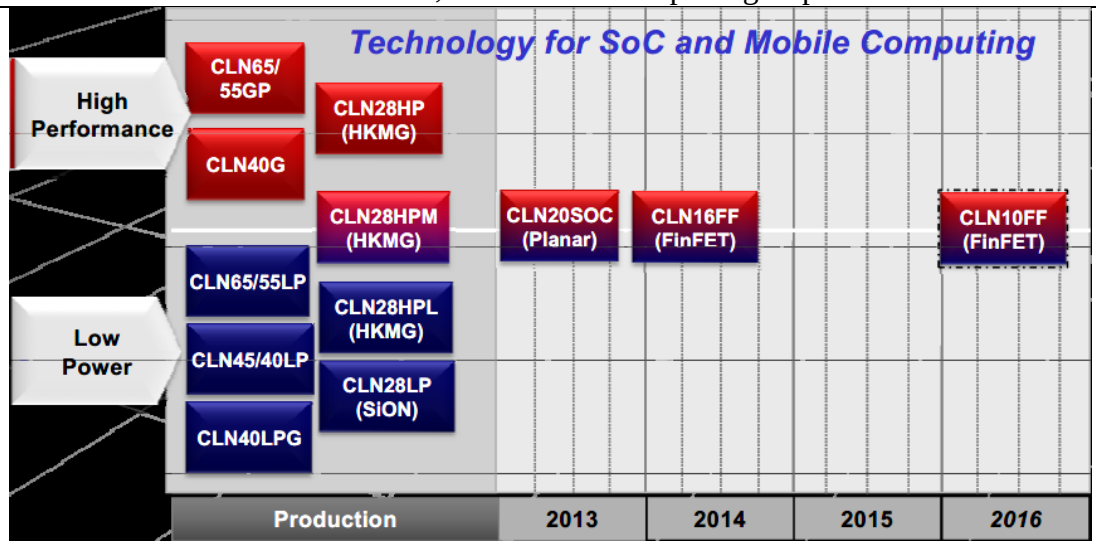
U.S. Patent No. 6,797,572: Claim 1

"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"

1. A method for forming a field effect transistor over a substrate, said method comprising steps of:	Integrated circuits manufactured using TSMC's 20nm and 28nm High-K Metal Gate (HKMG) process node (the "TSMC Product") are manufactured using a method of forming a field effect transistor over a substrate. For example, the Mstar MSDURP1602 integrated circuit (the "Mstar Chip") is an exemplary TSMC Product.  *See e.g.*, TSMC28HKMG_008. The Mstar Chip is manufactured using TSMC's 28nm HPC process node. Allwinner's octa-core A83 application processor is one of those fabricated in 28HPC. Amlogic's S812 4K HEVC modem, containing quad-core Cortex-A9 and T450 Mali GPU is another. MStar is using 28HPC for 4K ultrahigh definition television processor and Spreadtrum is offering smartphone ICs using the technology. *See e.g.*, TSMC Shrinks 28nm CMOS Process, https://electronics360.globalspec.com/article/4553/tsmc-shrinks-28nm-cmos-process. TSMC's high performance technology nodes, including HP, HPL, and HPM, and HPC use high-k metal gate (HKMG) gate-last technology.

U.S. Patent No. 6,797,572: Claim 1

"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"



See Henry Hsieh, TSMC Technology and Innovation Platform for Mobile Computing (Nov., 2012), p.3, *available at* http://www.armtechforum.com.cn/2012/10_TSMC.pdf; TSMC, TSMC 28nm Technology in Volume Production, *available at* https://www.tsmc.com/uploadfile/ir/BusinessRelease/20111024161709877_sw3I/Oct24_2011_E.pdf.

The 28HPC process, which has a high-k metal gate structure, can produce a 10 percent smaller die and 30 percent lower power consumption than the established 28LP process based on a silicon-oxynitride (SiON) gate insulator. So far 10 customers have taped out 28HPC IC designs and several of these have started volume production, TSMC said.

See e.g., TSMC Shrinks 28nm CMOS Process, https://electronics360.globalspec.com/article/4553/tsmc-shrinks-28nm-cmos-process.

U.S. Patent No. 6,797,572: Claim 1

"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"

	TSMC became the first foundry to provide the world's first 28nm General Purpose process technology in 2011 and has been adding more options ever since. TSMC provides customers with foundry's most comprehensive 28nm process portfolio that enable products that deliver higher performance, save more energy savings, and are more eco-friendly. TSMC's 28nm process technology features high performance and low power consumption advantages plus seamless integration with its 28nm design ecosystem to enable faster time-to-market. The 28nm process technology supports a wide range of applications, including Central Processing Units (CPUs), graphic processors (GPUs), high-speed networking chips, smart phones, application processors (APs), tablets, home entertainment, consumer electronics, and the Internet of Things. TSMC's industry-leading 28nm process technology mainly uses High-k Metal Gate (HKMG) gate-last technology. Compared to the gate-first technology, the gate-last offering provides more advantages, including lower leakage current and better chip performance. *See e.g.*, TSMC, 28nm Technology, http://www.tsmc.com/english/dedicatedFoundry/technology/28nm.htm. TSMC Products share substantially similar structure, function, operation, and implementation with respect to the claims at issue. For example, the 20nm technology node is a die shrink of the 28nm HKMG technology node. So now the first shoe has dropped (must check where that metaphor came from!), and we have a TSMC-fabbed 20-nm part in-house. It is in the lab at the moment, and we are waiting for the analysis results. It will be interesting to see what changes TSMC has made from the 28-nm process; in general, I expect mostly a shrink of the latter process, with no change to the materials of the high-k stack, though maybe to the sequence. At 28-nm the high- k was put down first, before the dummy poly gate, and it makes sense to move that deposition to after poly gate removal. That way, the high-k layer does not have to suffer the poly formation and source-drain engineering process steps, saving it from quite a bit of thermal processing. *See e.g.*, Semiconductor Manufacturing & Design Community, "TSMC 20nm Arrives – The First Shoe Drops," https://semimd.com/chipworks/2014/07/21/tsmc-20nm-arrives-the-first-shoe-drops/.

U.S. Patent No. 6,797,572: Claim 1

"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"

Node	28	20
Transistor Type	Planar – bulk	Planar - bulk
Gate	HKMG	HKMG
Threshold voltages	4	4
Strain	DSL, eSiGe, SM	DSL, eSiGe, SM
Metal layers	10	10

DSL = Dual Stress Liner, SM = Stress Memorization,
eSiGe = embedded Silicon Germanium

See e.g., IC Knowledge TSMC Structural Parameters, https://www.semiwiki.com/forum/attachments/content/attachments/18720d1481580837-tsmc-structure.pdf.

U.S. Patent No. 6,797,572: Claim 1

"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"

Foundry roadmap example - TSMC

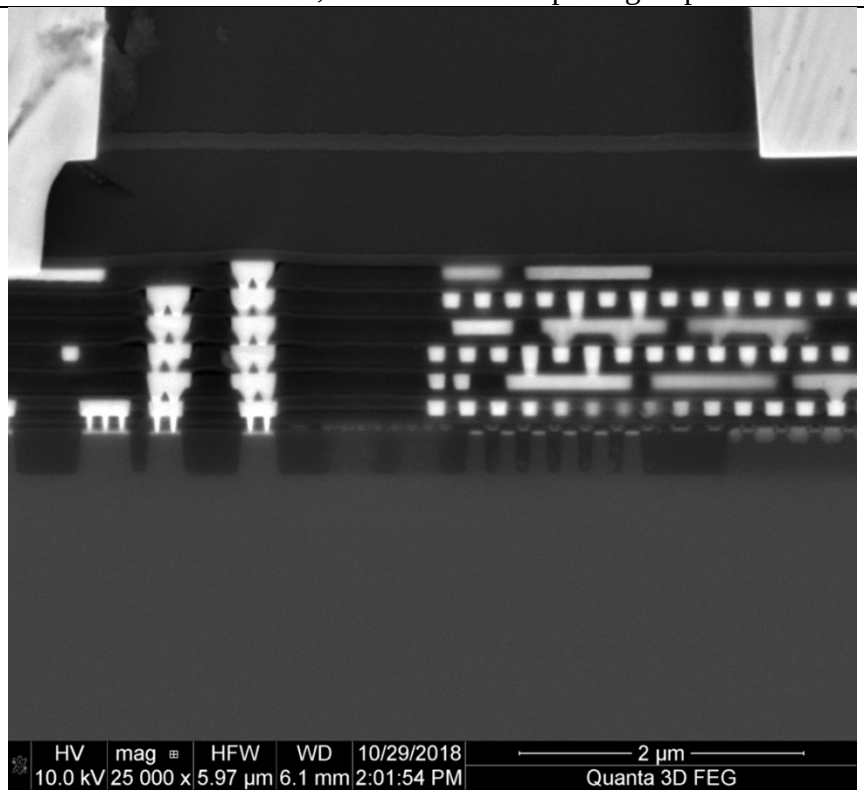
	28nm	20nm
Year	2011	2014
Transistor	Planar	Planar
Channel (NMOS/PMOS)	Si/Si	Si/Si
Threshold voltages	4	4
Metal layers	10	10
Contact and Via – Interconnect	W – Cu/Ta/TaN	W – Cu/Ta/TaN
Strain	DSL, eSiGe, SM	DSL, eSiGe, SM
CPP (nm)	113	90
MMP (nm)	90	64

See e.g., Technology and Cost Trends at Advanced Nodes, IC Knowledge, pg. 6, https://www.icknowledge.com/news/Technology%20and%20Cost%20Trends%20at%20Advanced%20Nodes%20-%20Revised.pdf.

The TSMC Product comprises field effect transistors (FETs) formed over a substrate. For example, the Mstar Chip comprises FETs formed ever a substrate.

U.S. Patent No. 6,797,572: Claim 1

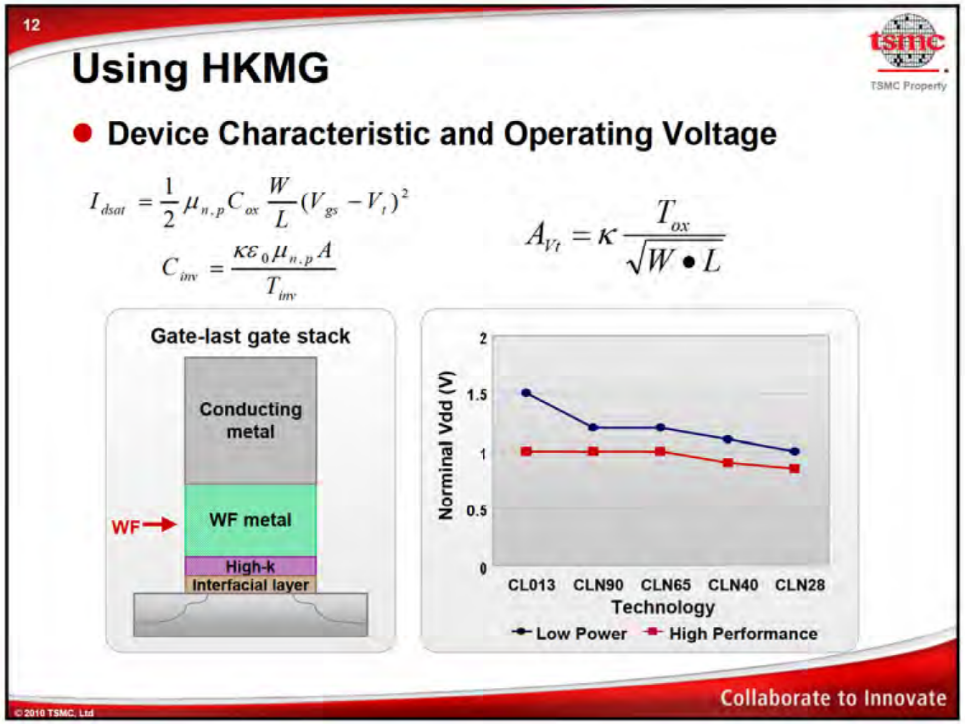
"1. A method for forming a field effect transistor over a substrate, said method comprising steps of:"



See e.g., TSMC28HKMG_010.

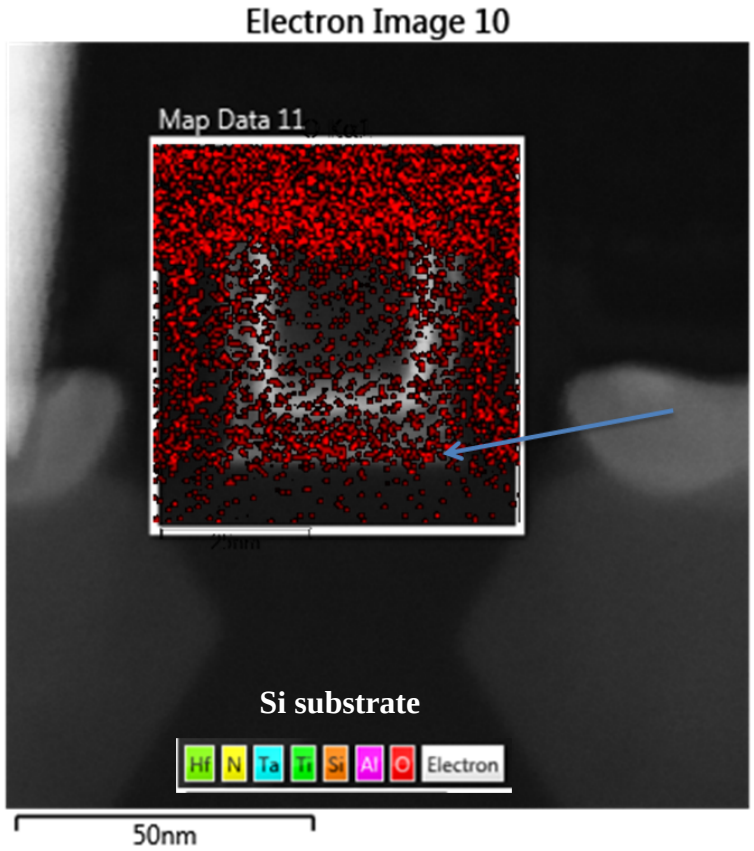
U.S. Patent No. 6,797,572: Claim 1

"forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness;"

forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness;	The TSMC Product is manufactured using the step of forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness. For example, in the Mstar Chip, an interfacial layer is formed as shown below.  *See e.g.*, TSMC 2010 Technology Symposium ("2010 Symposium"), p. 54. Furthermore, the Mstar Chip comprises an interfacial oxide layer formed over the channel region of the silicon substrate. Energy Dispersive X-ray spectroscopy (EDS) compositional samples from the silicon substrate to the middle of the gate electrode show that there is a thin oxide layer above the silicon substrate.

U.S. Patent No. 6,797,372: Claim 1

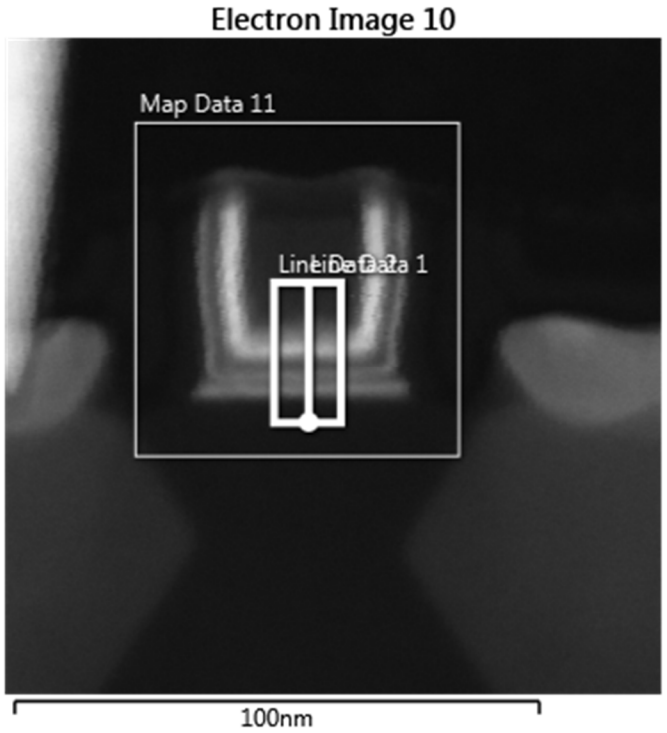
"forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness;"



See e.g., TSMC28HKMG_012.

U.S. Patent No. 6,797,372: Claim 1

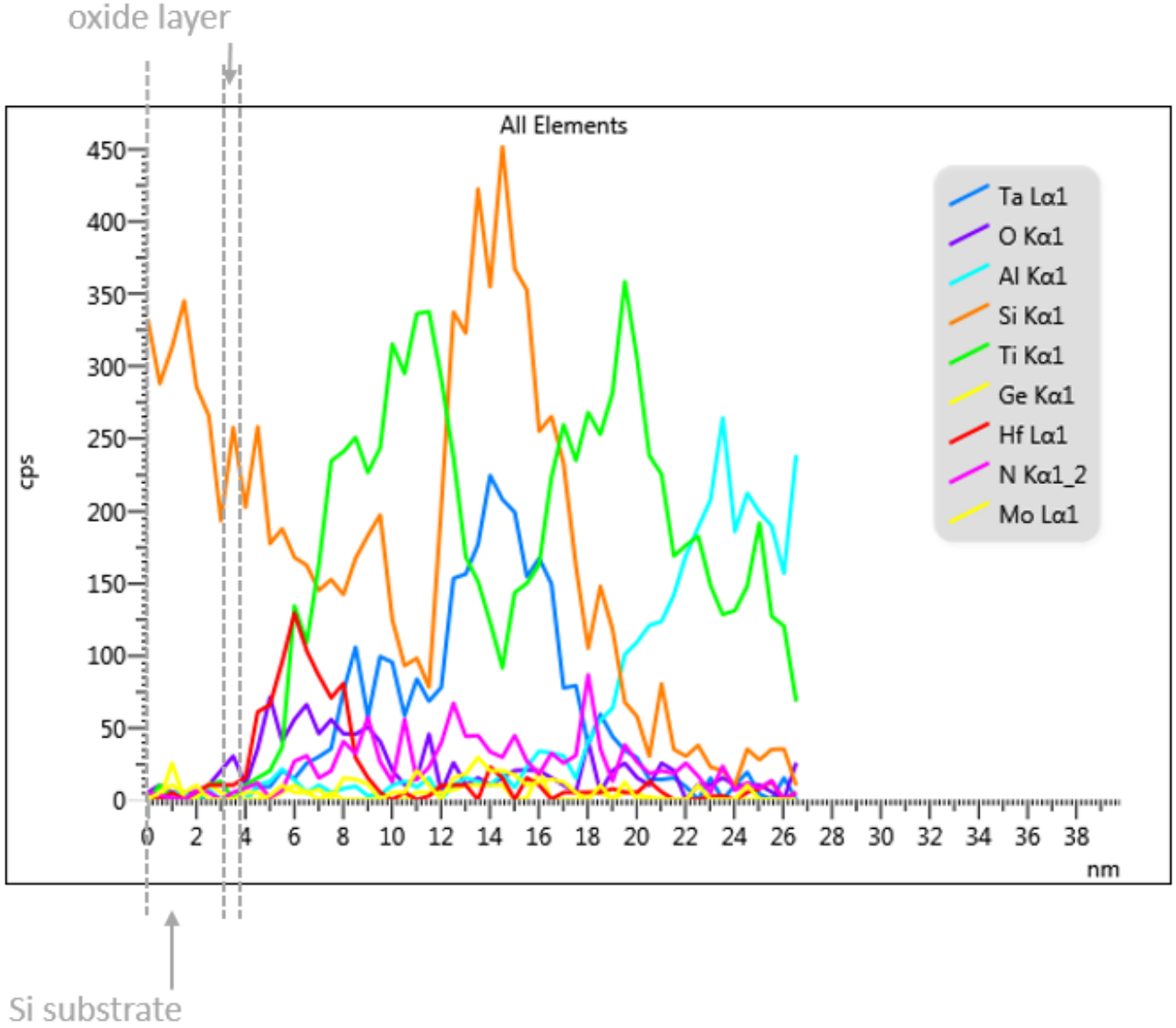
"forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness;"



See e.g., TSMC28HKMG_017.

U.S. Patent No. 6,797,372: Claim 1

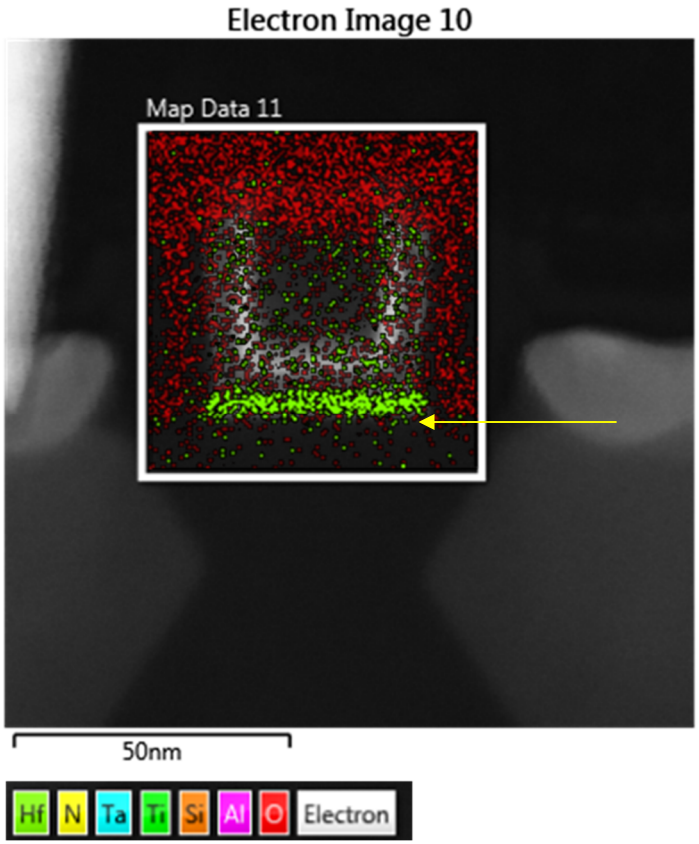
"forming an interfacial oxide layer over a channel region of said substrate, said interfacial oxide layer having a first thickness;"



See e.g., TSMC28HKMG_017.

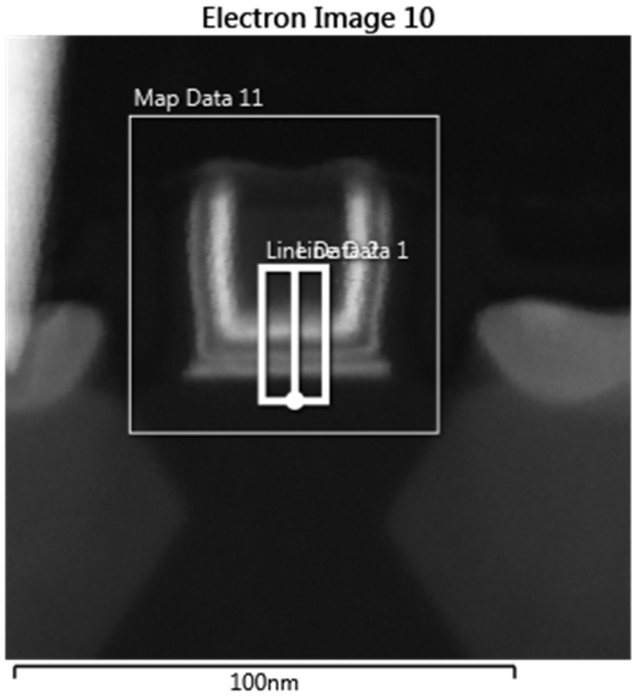
U.S. Patent No. 6,797,372: Claim 1

"forming an oxygen-attracting layer over said interfacial oxide layer;"

forming an oxygen-attracting layer over said interfacial oxide layer;	The TSMC Product is manufactured using the step of forming an oxygen-attracting layer over the interfacial oxide layer. For example, as shown below, the Mstar Chip contains a layer of Hafnium and Hafnium Oxide over the interfacial oxide layer. EDS compositional samples from the silicon substrate to the middle of the gate electrode show that there is a thin oxygen attracting layer between the oxide layer and the high-K dielectric layer. In particular, as illustrated below, the hafnium signal begins to rise near the oxygen attracting layer region and a local oxygen peak closely follows.  *See e.g.*, TSMC28HKMG_012.

U.S. Patent No. 6,797,372: Claim 1

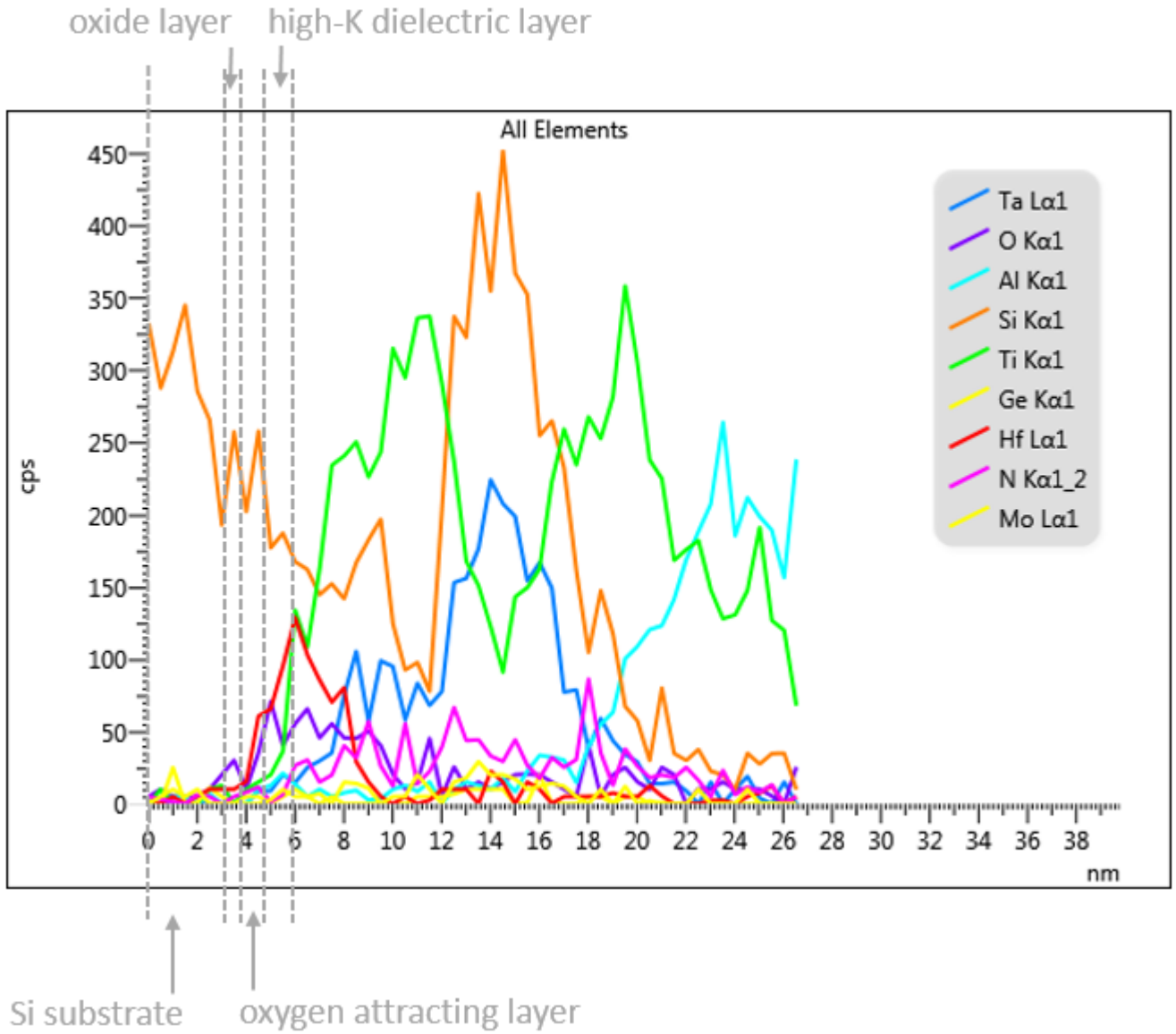
"forming an oxygen-attracting layer over said interfacial oxide layer;"



See e.g., TSMC28HKMG_017.

U.S. Patent No. 6,797,372: Claim 1

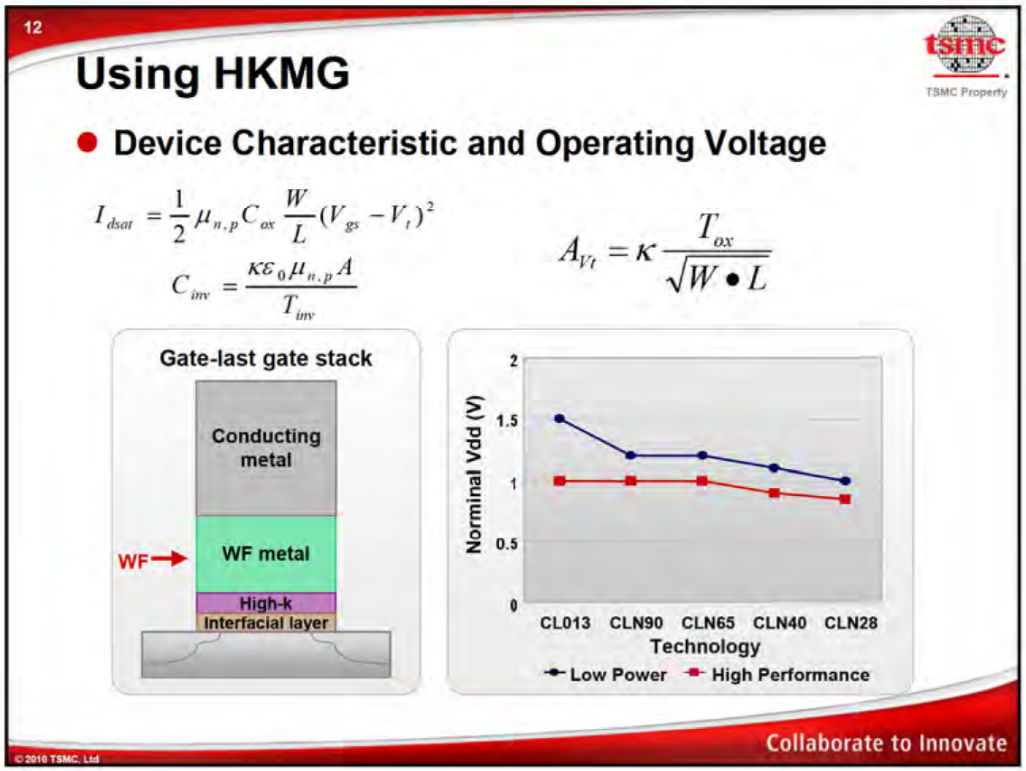
"forming an oxygen-attracting layer over said interfacial oxide layer;"



See e.g., TSMC28HKMG_017.

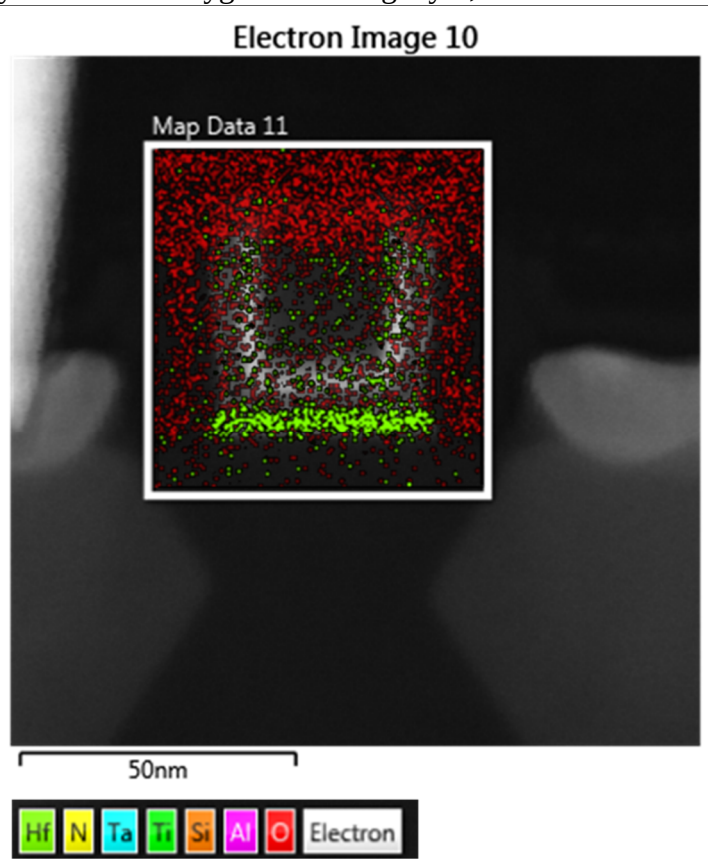
U.S. Patent No. 6,797,572: Claim 1

"forming a high-k dielectric layer over said oxygen-attracting layer;"

forming a high-k dielectric layer over said oxygen-attracting layer;	The TSMC Product is manufactured using the step of forming a high-k dielectric layer over said oxygen-attracting layer. For example, a high-K dielectric layer is formed as shown below.  *See e.g.*, 2010 Symposium p. 54. Furthermore, as shown below, there is a layer of Hafnium Oxide over the oxygen-attracting layer in the Mstar Chip. EDS compositional samples from the silicon substrate to the middle of the gate electrode show that there is a HfO layer over the oxygen-attracting layer.

U.S. Patent No. 6,797,372: Claim 1

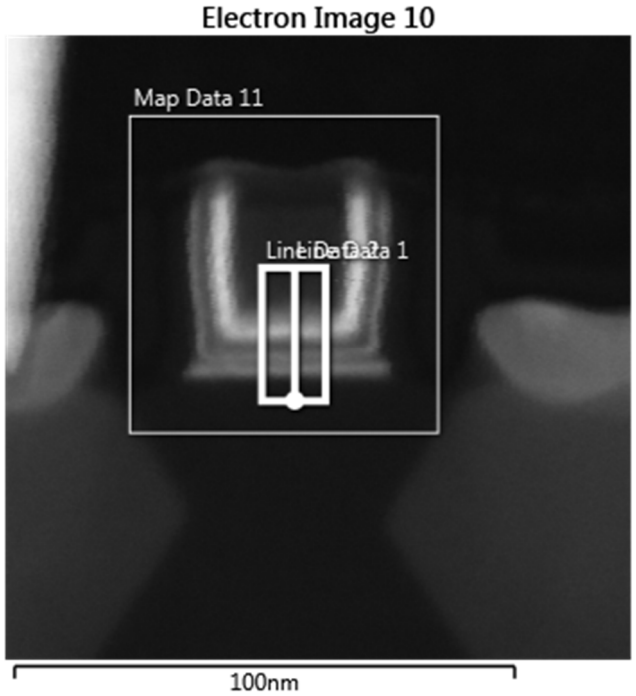
"forming a high-k dielectric layer over said oxygen-attracting layer;"



See e.g., TSMC28HKMG_012.

U.S. Patent No. 6,797,372: Claim 1

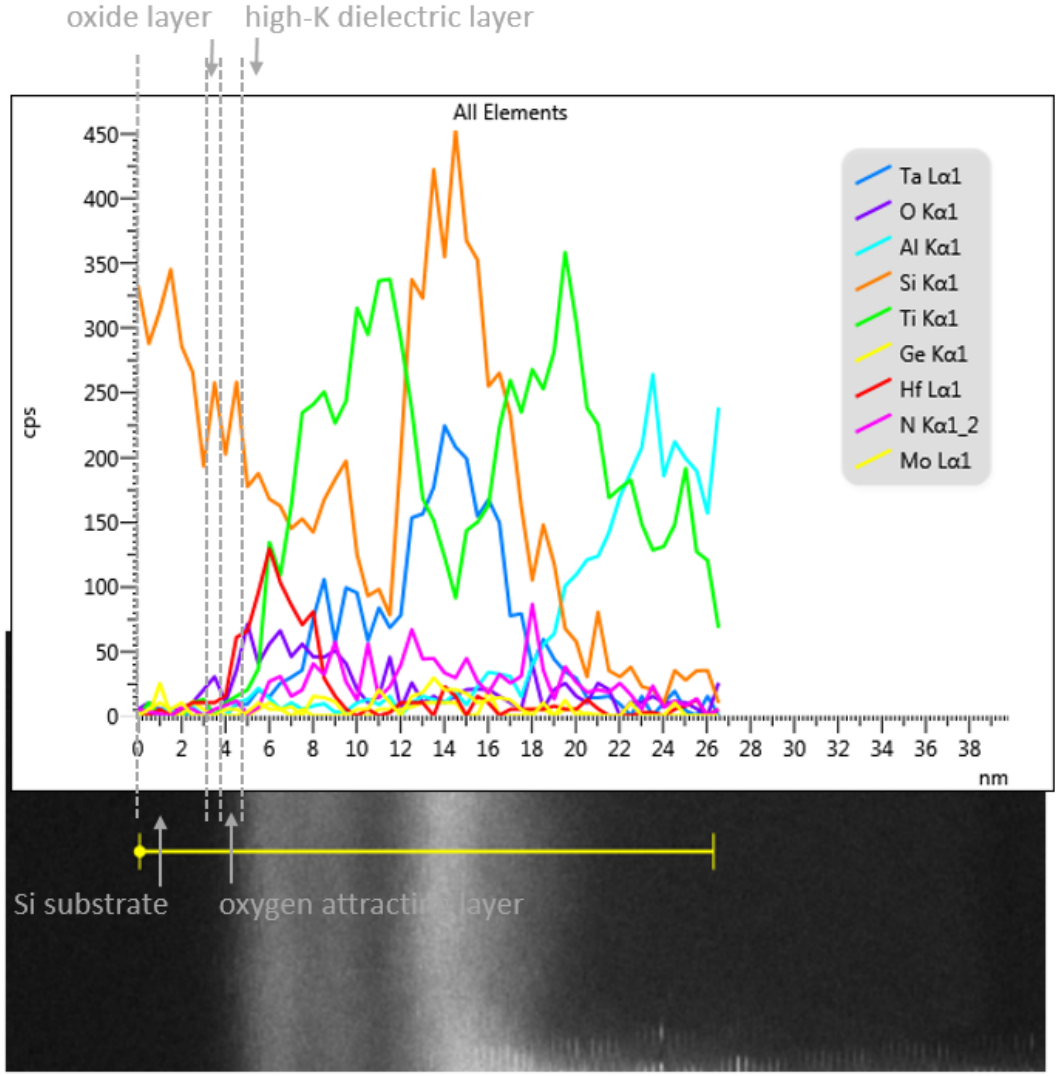
"forming a high-k dielectric layer over said oxygen-attracting layer;"



See e.g., TSMC28HKMG_017.

U.S. Patent No. 6,797,372: Claim 1

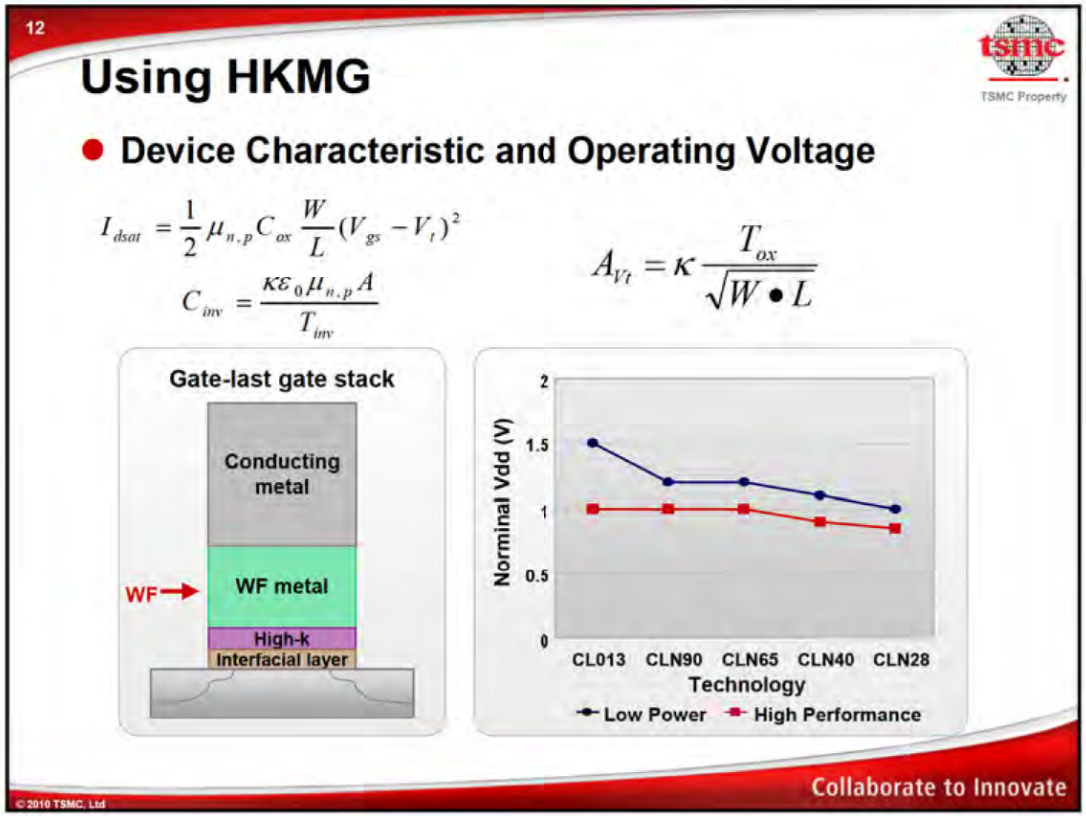
"forming a high-k dielectric layer over said oxygen-attracting layer;"



See e.g., TSMC28HKMG_017.

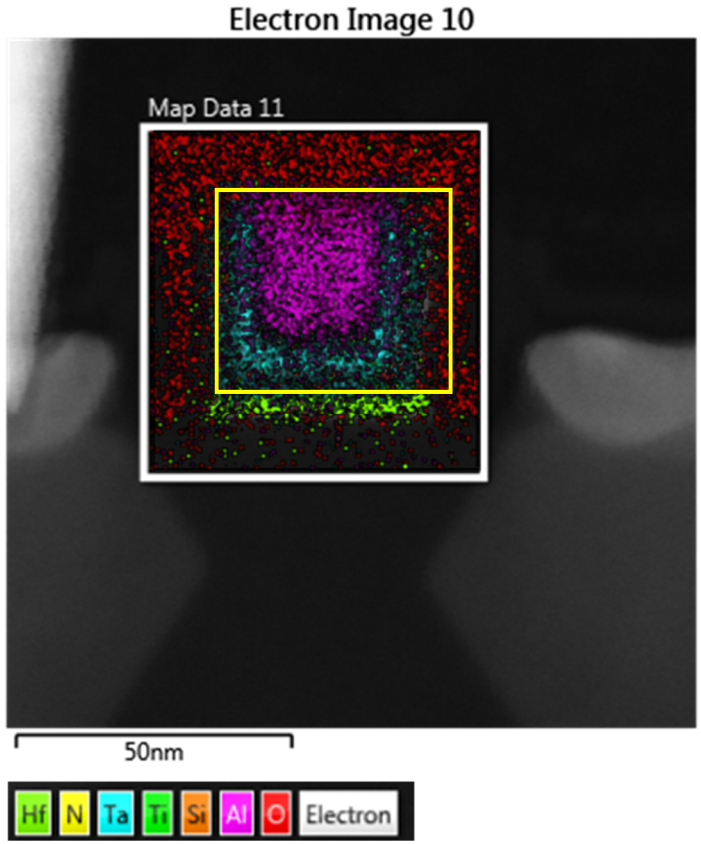
U.S. Patent No. 6,797,372: Claim 1

"forming a gate electrode layer over said high-k dielectric layer;"

forming a gate electrode layer over said high-k dielectric layer;	The TSMC Product is manufactured using the step of forming a gate electrode layer over the high-k dielectric layer. For example, a gate electrode is formed over the high-K dielectric layer as shown below.  *See e.g.*, 2010 Symposium, p. 54. Furthermore, the gate electrode layer (boxed in yellow) is formed above the high-K dielectric layer in the Mstar Chip. EDS compositional samples from the silicon substrate to the middle of the gate electrode show that the gate electrode comprises Titanium, Tantalum and Aluminum.

U.S. Patent No. 6,797,372: Claim 1

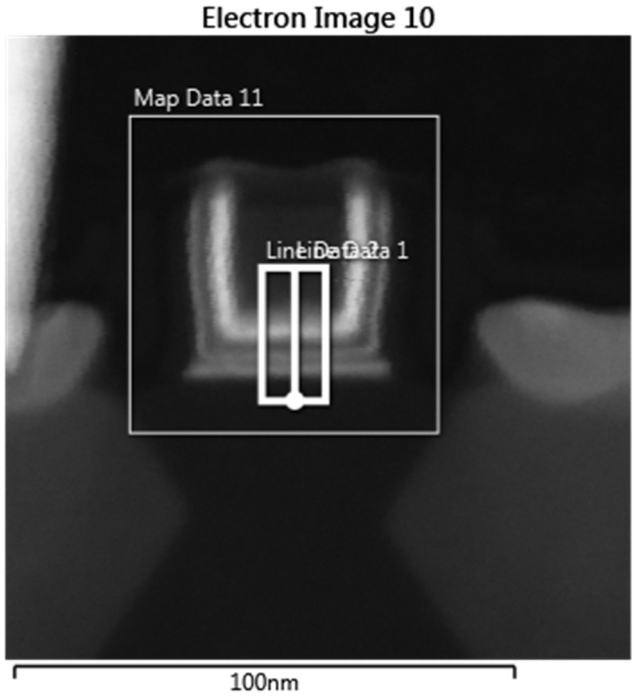
"forming a gate electrode layer over said high-k dielectric layer;"



See e.g., TSMC28HKMG_012.

U.S. Patent No. 6,797,372: Claim 1

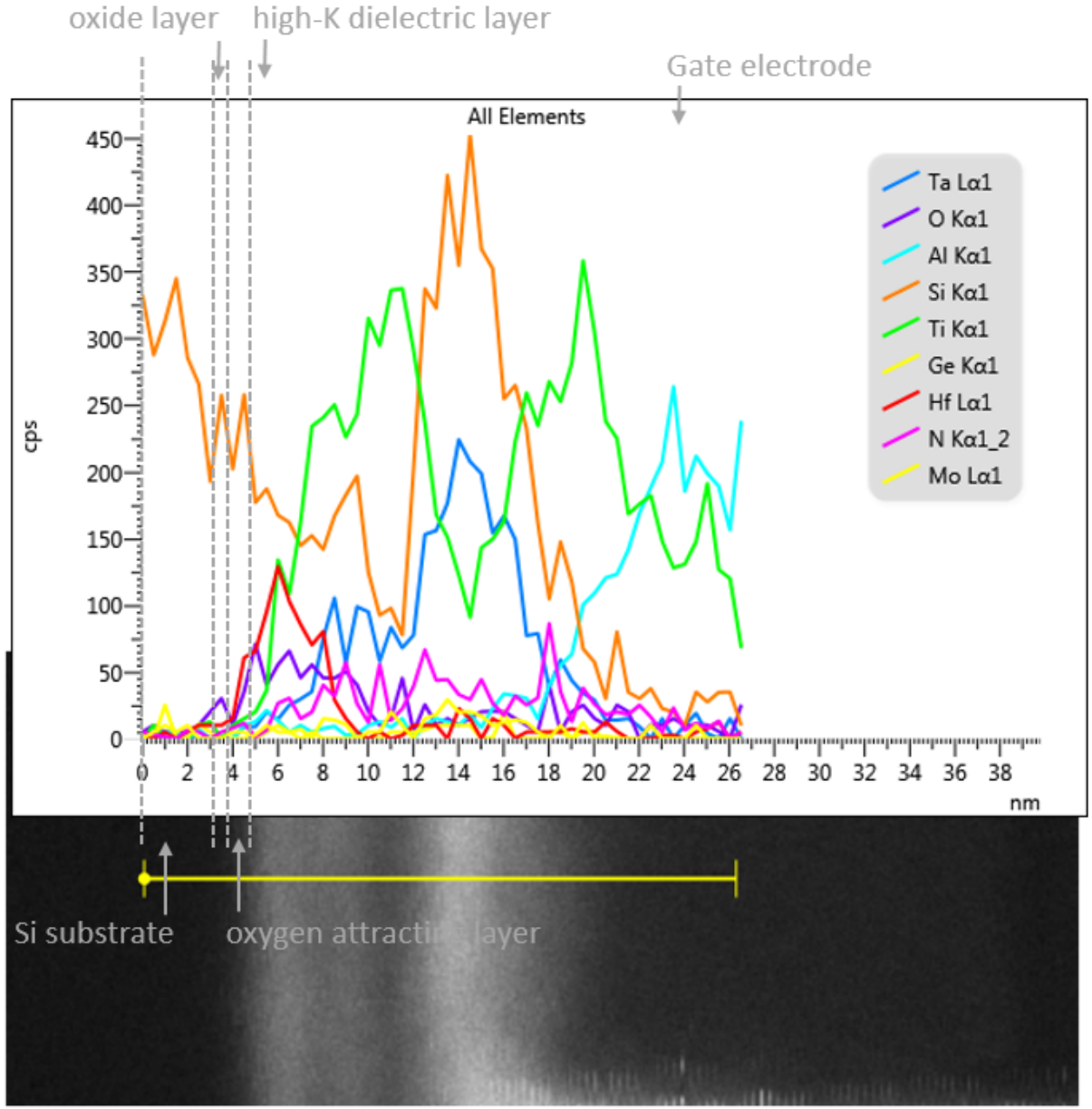
"forming a gate electrode layer over said high-k dielectric layer;"



See e.g., TSMC28HKMG_017.

U.S. Patent No. 6,797,372: Claim 1

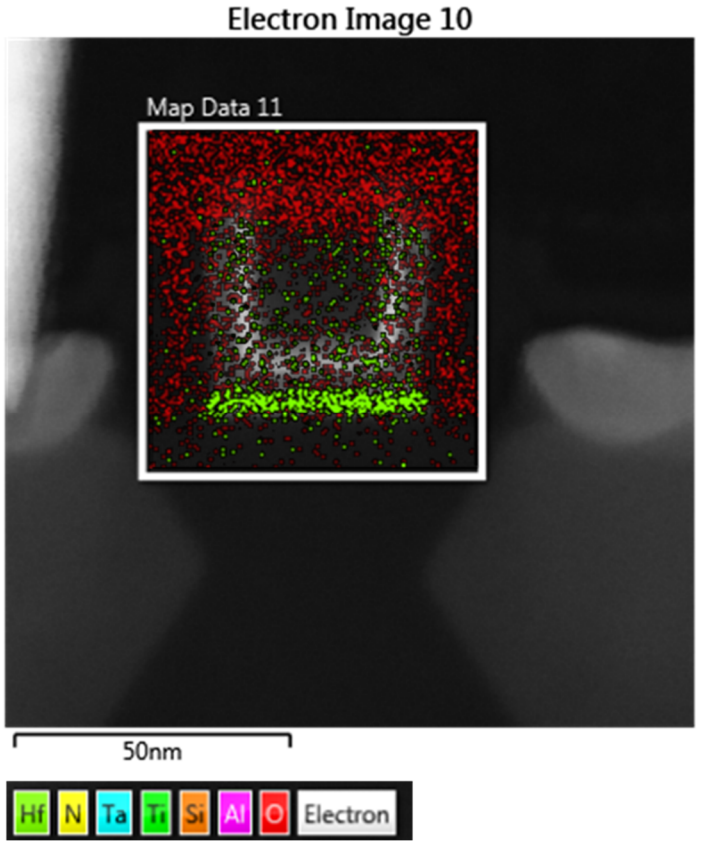
"forming a gate electrode layer over said high-k dielectric layer;"



See e.g., TSMC28HKMG_017.

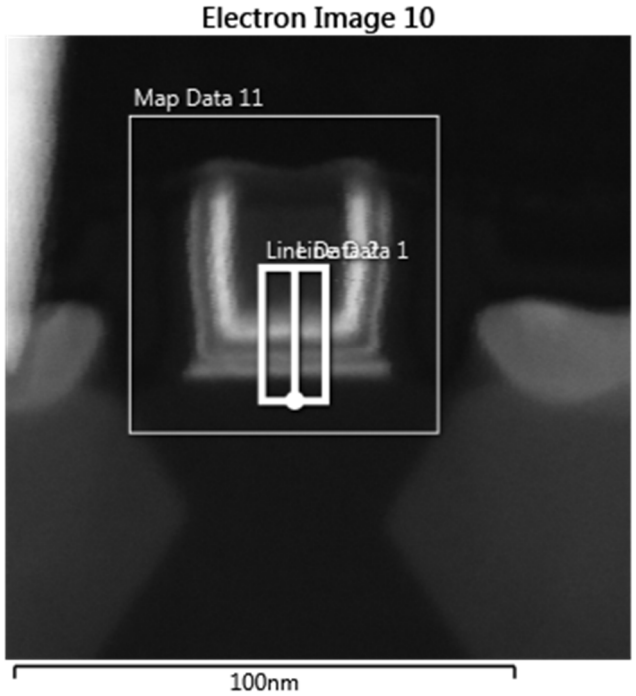
U.S. Patent No. 6,797,572: Claim 1

"wherein said oxygen-attracting layer prevents said first thickness of said interfacial oxide layer from increasing."

wherein said oxygen-attracting layer prevents said first thickness of said interfacial oxide layer from increasing.	Upon information and belief, the oxygen attracting layer prevents said first thickness of said interfacial oxide layer from increasing.  *See e.g.*, TSMC28HKMG_012.

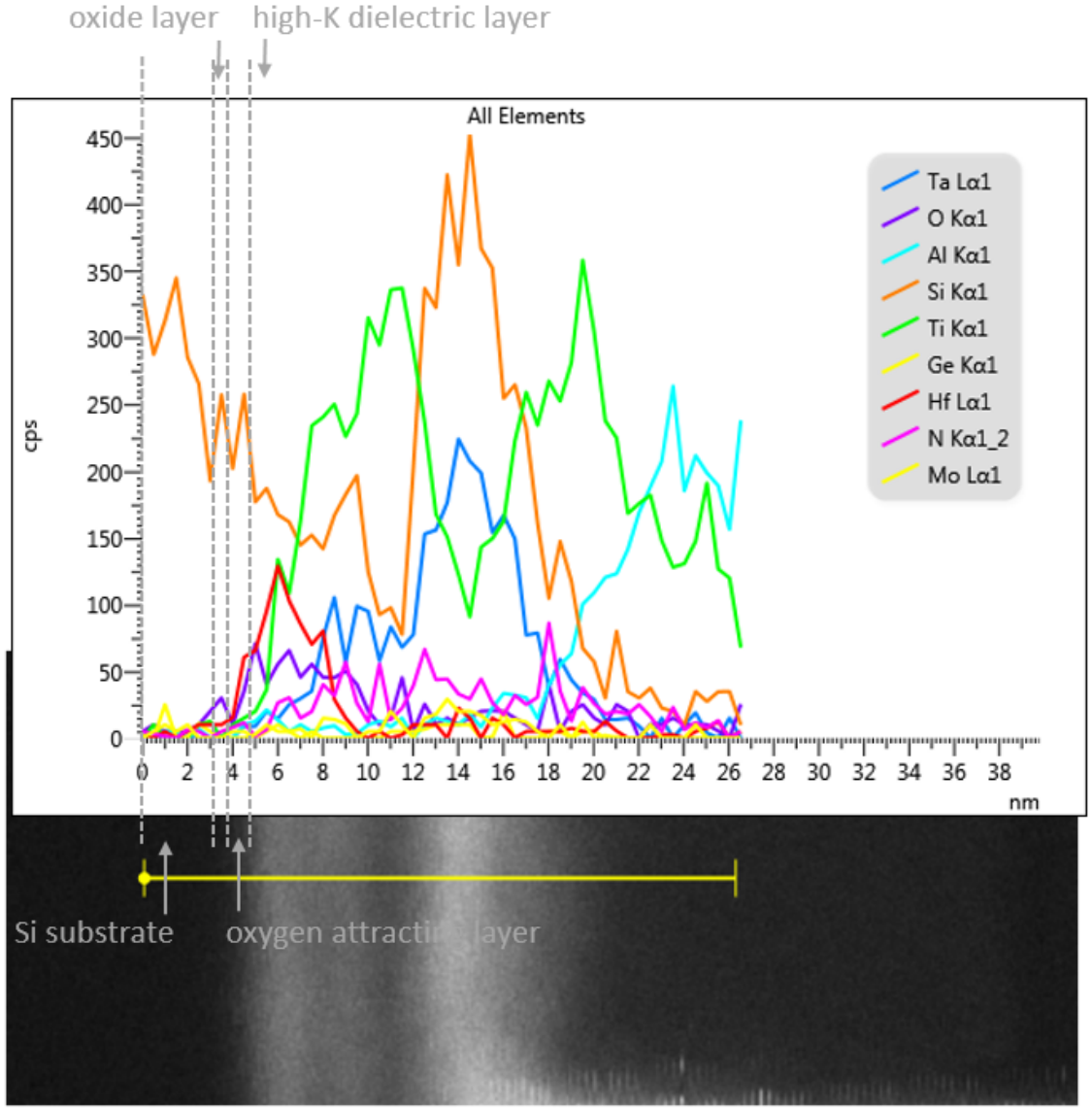
U.S. Patent No. 6,797,572: Claim 1

"wherein said oxygen-attracting layer prevents said first thickness of said interfacial oxide layer from increasing."

	 *See e.g.*, TSMC28HKMG_017.

U.S. Patent No. 6,797,572: Claim 1

"wherein said oxygen-attracting layer prevents said first thickness of said interfacial oxide layer from increasing."



See e.g., TSMC28HKMG_017.